AMENDMENTS TO THE SPECIFICATION

Please amend the first paragraph on page 7, lines 1-7 as shown.

One embodiment of the invention is described with particularity with respect to Figure 1. Figure 1 shows a block diagram of an integrated circuit device 101, or system-on-chip (SOC) mentioned above. This circuit may include a processor 102 and debug circuit[[193]] 103 or module interconnected by a system bus 105. System bus 105 may be, for example, a conventional processor bus, packet switch, or other communication medium used to communicate operating information between modules of device 101. Operations such as

Please amend the fourth paragraph on page 18, lines 21 through 28 as shown.

Further, branch unit 507 may provide ASID information Sr.asid 515 every time that there is an ASID update. In one embodiment of the invention, ~~sr.asid~~ Sr.asid signal 515 is multiplexed with operand address watchpoint information 523 to produce p_dm_data 516. In one embodiment, there can be no clash between the transmission of ASID information and other trace data, because ASID updates occur after a return from exception (RTE) instruction reaches the writeback stage of execution. Because the RTE instruction is a back-serialized instruction, there will be no instructions in the pipeline until after the RTE instruction has completed.